Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

- (currently amended) A DRAM cell comprising:
 - a semiconductor substrate;
 - a trench extending into the substrate;
 - a cell capacitor disposed in a bottom portion of the trench;
 - a cell transistor disposed in a top portion of the trench above the cell capacitor;
 - a node conducting element connecting the cell capacitor to the cell transistor; and
- a collar disposed about the node conducting element between the cell transistor and the cell capacitor;

wherein:

the collar is disposed in the substrate, at least partially outside of the trench, between the cell capacitor and the cell transistor;

further comprising;

a strap disposed in the trench and having an outside peripheral surface; and the collar is laterally adjacent and surrounds the outside peripheral surface of the buried strap.

- (original) A DRAM cell, according to claim 1, wherein:
 the collar is disposed substantially outside of the trench.
- (original) A DRAM cell, according to claim 1, wherein:
 the collar is disposed wholly outside of the trench
- 4. (original) A DRAM cell, according to claim 1, further comprising:a strap disposed between the node conducting element and the cell transistor.

- 5. (original) A DRAM cell, according to claim 1, further comprising: a strap which is self-aligned with the collar.
- 6. (original) A DRAM cell, according to claim 1, further comprising:a strap disposed in the trench at substantially a same depth as the collar.
- (original) A DRAM cell, according to claim 1, further comprising:
 a strap disposed in the trench and laterally surrounded by the collar.
- 8. (canceled) A DRAM cell, according to claim 1, further comprising:

 a strap disposed in the trench and having a periphery; and
 the cellar is laterally adjacent and surrounds the periphery of the buried strap.
- 9. (currently amended) A DRAM cell, according to claim 1, comprising:

 a semiconductor substrate;

 a trench extending into the substrate;

 a cell capacitor disposed in a bottom portion of the trench;

 a cell transistor disposed in a top portion of the trench above the cell capacitor;

 a node conducting element connecting the cell capacitor to the cell transistor; and
 a cellar disposed about the node conducting element between the cell transistor and the
 cell capacitor; and

a strap;

wherein:

the strap is embedded into a top surface of the collar.

- A DRAM cell, according to claim 9, wherein:
 the strap extends no higher than the collar.
- 11. (canceled) A DRAM cell, according to claim 9, wherein:

the strap is has a periphery which is laterally surrounded by the collar.

12. (currently amended) A method of forming DRAM cells, comprising:
forming trenches in a semiconductor substrate;
forming cell capacitors in a bottom portion of the trench;
forming cell transistors in a top portion of the trench; and
for each DRAM cell, providing a collar between the cell capacitor and the cell transistor,
the collar being disposed in the substrate, at least partially outside of the trench;
for each DRAM cell, forming a recess in a top inside corner of the collar; and
for each DRAM cell, embedding a strap in the recess.

- 13. (currently amended) A method, according to claim 12, wherein: the collar is disposed at least substantially outside of the trench.
- 14. (currently amended) A method, according to claim 12, wherein: the collar is disposed wholly outside of the trench.
- 15. (canceled) A method, according to claim 12, further comprising:
 for each DRAM cell, providing a node conducting element between the cell capacitor and the cell-transistor;

wherein:

the collar is disposed laterally adjacent the node poly element.

16. (canceled) A method, according to claim 12, further comprising:
for each DRAM cell, providing a node conducting element between the cell capacitor and the cell transistor;

wherein:

the collar surrounds a periphery of the node pely element.

- 17. (canceled) A method, according to claim 12, further comprising:

 for each DRAM cell, providing a node conducting element between the cell capacitor and the cell transistor; and

 a strap disposed between the node conducting element and the cell transistor.
- 18. (canceled) A method, according to claim 12, further comprising:

 for each DRAM cell, providing a strap which is self-aligned with the collar.
- 19. (currently amended) A method, according to claim 12, [further comprising:
 for each DRAM cell, disposing a strap in the trench at substantially a same depth as the
 collar]
 wherein the strap extends no higher than the collar.
- 20. (original) A method, according to claim 12, further comprising: for each DRAM cell, disposing a strap in the trench; and the strap is laterally surrounded by the collar.

Please enter the following:

- 21. (new) A DRAM cell, according to claim 1, further comprising: a recess disposed in a top inside corner of the collar; and the strap extends into the recess in the top inside corner of the collar.
- 22. (new) A DRAM cell, according to claim 1, wherein: the strap is fully vertically embedded in the collar and it is laterally surrounded by the collar.
- 23. (new) A DRAM cell, according to claim 1, wherein: the strap is disposed in the trench at substantially a same depth as the collar; and

the collar extends deeper into the trench than the strap and and covers a bottom surface of the strap.

- 24. (new) A DRAM cell, according to claim 1, wherein: the collar covers a bottom surface of the strap.
- 25. (new) A method, according to claim 12, wherein:
 constraining outward diffusion of the strap by the laterally-surrounding collar; and
 constraining downward diffusion of the strap with the collar.
- 26. (new) A method, according to claim 12, wherein:an upper surface of the buried strap does not extend above an upper surface of the collar.